

sidekiq™ X2

High Performance Multi-Channel RF Transceiver in VITA 57.1 (FMC) Form Factor



KEY FEATURES

- » VITA 57.1 FPGA Mezzanine Card (FMC) with high pin count (HPC) interface
- » Two phase coherent RF receivers (common LO) + third independently tunable RF receiver
- » Two phase coherent RF transmitters (common LO)
- » Continuous RF tuning range between 1 MHz and 6 GHz
- » Configurable RF channel bandwidth up to 100 MHz per channel
- » Exceptional dynamic range with 16-bit A/D and 14-bit D/A converters
- » Thunderbolt™ 3 and 3U/6U VPX deployment options with COTS carriers

Epiq Solutions' Sidekiq X2 multi-tuner RF transceiver card defines the state of the art in high performance flexible RF. Based on Analog Devices' AD9371 wideband transceiver, the X2 achieves unprecedented levels of RF performance to provide a production ready RF transceiver solution in a VITA 57.1 FPGA Mezzanine Card (FMC) compliant form factor. Sidekiq X2 includes additional features to extend the RF tuning range of the AD9371, while also integrating Rx pre-select filtering and clock synchronization to support real world deployment use cases.

Sidekiq X2 supports lab and field deployments with a COTS FPGA carrier card integrated into a Thunderbolt™ 3 chassis. For ruggedized deployments, Sidekiq X2 can be integrated into COTS 3U or 6U VPX carrier cards. Both conduction and convection cooled options are supported. The Sidekiq X2 Platform Development Kit (PDK) provides customers with access to both a software API for interfacing to the card, as well as the source code for the FPGA reference design targeting a Xilinx Kintex® UltraScale™ XCKU060 device.

Thunderbolt 3 Development Kit



RF RECEIVER SPECIFICATION

Number of Phase Coherent Receivers

2 with SSMC interfaces

Number of Additional Independently Tunable Receivers

1 with SSMC interface

RF Tuning Range

1 MHz to 6 GHz

RF Tuning Step Size

< 5 Hz

RF Channel Bandwidth

Up to 100 MHz

Typical Rx Noise Figure

8 dB

Typical Input IP3 (at 8 dB noise figure)

+8 dBm

Max A/D Converter Sample Rate

122.88 Msamples/sec

A/D Converter Sample Width

16 bits

Rx Gain Modes

Manual or automatic (AGC)

Pre-Select Filter

Seven bandpass RF filters on each RF receiver

RF TRANSMITTER SPECIFICATION

Number of Phase Coherent Transmitters

2 with SSMC interfaces

RF Tuning Range

Tx1 - 1 MHz to 6 GHz

Tx2 - 300 MHz to 6 GHz

RF Tuning Step Size

< 5 Hz

RF Channel Bandwidth

Up to 100 MHz

Typical RF Output Power

Up to +5 dBm

Max D/A Sample Rate

122.88 Msamples/sec

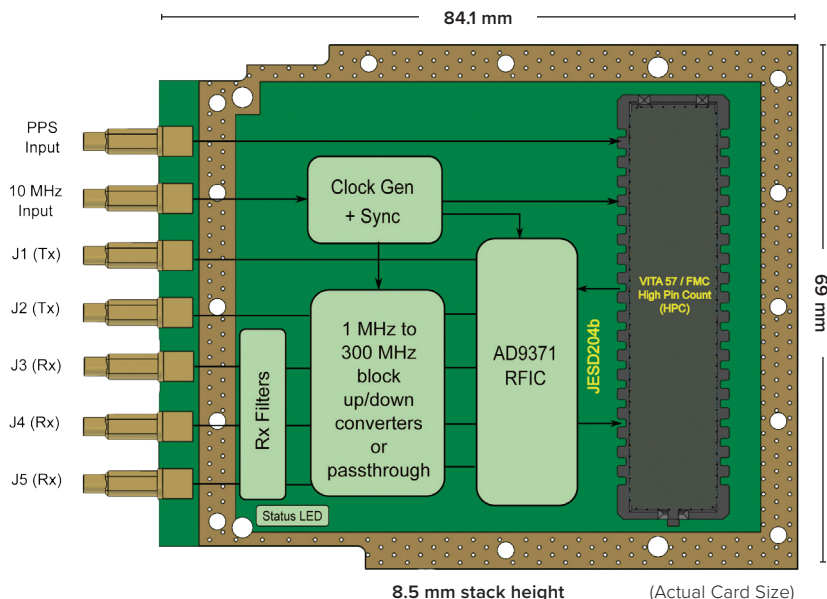
D/A Converter Sample Width

14-bits

*All specifications are subject to change without notice.

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BLOCK DIAGRAM



DIGITAL SPECIFICATION

A/D and D/A interface to Host System

JESD204b

Additional I/O from Host

I2C + singled-ended GPIO

PPS Interface

SSMC

PPS Input

Direct to host system FPGA (for timestamping)

10 MHz Reference Input Interface

SSMC

10 MHz Reference Input

For phase locking card to external system

MECHANICAL SPECIFICATION

Form Factor

VITA57.1 High Pin Count FPGA Mezzanine Card (FMC)

Thermal Management

Convection cooled (conduction option on request)

Typical Power Consumption

4-10 Watts (depending on # of channels in use)

Component Temperature Rating

-40 to +85 degrees C

For more information about Sideiq X2 and the available Development Kit options, please contact Epiq Solutions.